INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
63979-029	**10/626,642**
APPLICANT: **Takeshi TAKAGI**	
FILING DATE: **July 25, 2003**	GROUP

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EM		US	5,512,771	04/30/1996	Hiroki et al.	
EM		US	2002/0005581 A1	01/17/2002	Kurata	
		US				
		US				
		US				
		US				
		US				
		US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
EM		JP 62-045071	02/27/1987	NEC CORP		(Japan w/English Abstract)	
		JP P2001-119026A	04/27/2001	SAMSUNG ELECTRONICS CO LTD		(Japan w/English Abstract)	
		JP 9-45903	02/14/1997	MATSUSHITA ELECTRIC IND CO LTD		(Japan w/English Abstract)	
		JP 3-69166	03/25/1991	NIPPON SOKEN INC		(Japan w/English Abstract)	
		JP 6-267972	09/22/1994	NEW JAPAN RADIO CO LTD		(Japan w/English Abstract)	
		JP P2002-100768A	04/05/2002	FUJITSU LTD		(Japan w/English Abstract)	
EM		JP 9-148564	06/06/1997	NEC CORP		(Japan w/English Abstract)	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate),of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
EM		Wen-Chin LEE, et al., "Investigation of Poly-$Si_{1-x}Ge_x$ for Dual-Gate CMOS Technology", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998
		T. GHANI, et al., "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", 1999 IEEE pp. 415-418
EM		T. SKOTNICKI, et al., "Well-Controlled, Selectively Under-Etched Si/SiGe Gates for RF and High Performance CMOS", 2000 IEEE

EXAMINER	DATE CONSIDERED
EM	7-5-04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.